

# Thomas Block

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## EDUCATION

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### University of Notre Dame | Notre Dame, IN

*B.S. Electrical Engineering, Minor in Engineering Corporate Practice*

Active DoD Secret Security Clearance (2026)

Expected May 2028

**GPA: 3.92**

Dean's List (All Semesters)

## EXPERIENCE

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### Lockheed Martin

*Systems Engineering Intern*

Moorestown, NJ

*Summer 2026*

- Test and validate embedded devices across multiple combat systems, translating hardware requirements into structured test protocols within a classified lab environment
- Build a Python/PyQt5 Linux dashboard powered by 8 automation scripts that aggregate simulation test outputs across configurations and flag program pass/fail compliance, cutting manual test review time
- Develop model-based systems engineering architectures in Cameo Systems Modeler for AEGIS supply chain and systems integration

### Snider Group, University of Notre Dame

*Undergraduate Researcher*

Notre Dame, IN

*Spring 2026 – Present*

- Designed and simulated a 32-bit logarithmic barrel shifter at the transistor level in Cadence Virtuoso using a 5-stage 2-to-1 mux cascade (shifts of 1, 2, 4, 8, 16) supporting both logical and arithmetic shift modes
- Replaced pass transistors with transmission gates and added buffered control lines to eliminate voltage droop, producing clean output across all 32 shift amounts
- Built the shifter as the first ALU datapath block for reversible adiabatic low-power computing research

### IrishSAT, University of Notre Dame

*Chief Thermal Engineer*

Notre Dame, IN

*Fall 2025 – Present*

- Lead a 5-person team designing thermal-control systems for a 200 cm<sup>3</sup> low-earth-orbit satellite
- Developed a 600-line C++ thermal model achieving 0.01°C onboard sensing accuracy

## TECHNICAL PROJECTS

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### RISC-V Soft-Core Processor & System Monitor | Verilog, FPGA (Artix-7), RISC-V, SPI, UART

- Designed a pipelined 32-bit RISC-V (RV32I) soft-core processor in Verilog on a Xilinx Artix-7 FPGA, with a 5-stage pipeline, hazard detection, and data forwarding running at 100 MHz
- Verified the core against the standard RISC-V test suite using self-checking testbenches and executed C programs compiled through the riscv-gcc toolchain
- Built a real-time system monitor on the core, ingesting host telemetry over UART and driving an SPI TFT to render live CPU, GPU, and memory statistics

### Embedded Thermostat Controller | PIC24, C, I<sup>2</sup>C, SPI, UART

Spring 2026

- Built a closed-loop thermostat controller on a PIC24 microcontroller in C, reading a DS1631 sensor over I<sup>2</sup>C and driving an LCD, RGB status LED, and dual-pushbutton setpoint interface across 4 peripheral subsystems
- Implemented interrupt-driven heat/cool control logic and a UART event-logging system that records all temperature changes and user inputs for real-time serial monitoring

## LEADERSHIP

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### Morrissey Hall

*President*

Notre Dame, IN

*Spring 2026 – Present*

- Elected to represent 180+ residents; manage a \$40K budget across 8 committees and lead a \$30K alumni fundraising effort

### Student International Business Council

*Project Leader*

Notre Dame, IN

*Fall 2024 – Present*

- Led 8–10 student consulting teams on McKinsey and PwC engagements; placed 1st of 13 at Notre Dame in Deloitte's National Undergraduate Case Competition (top 16 of 173 nationally)

## TECHNICAL SKILLS

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**Languages:** Verilog, C/C++, Python, MATLAB, Assembly

**EDA & Hardware:** Cadence Virtuoso, LTspice, Cameo Systems Modeler, Arduino, Git, Linux